Faculty of Engineering & Technology
KAKATIYA UNIVERSITY, WARANGAL-506 009
Department of Electronics & Communication Engineering

B. Tech. (ECE)

III - SEMESTER

Sl. No.	Course Code	Course Title	Scheme of Instruction			Credits
			L	T	P	
1.	BSC 105	Mathematics – III	3	0	0	3
2.	HS 901 MB	Managerial Economics and Accountancy	3	0	0	3
3.	PC 301 EC	Electronics Devices and Circuits	3	1	0	4
4.	PC 302 EC	Digital System Design	3	1	0	4
5.	PC 303 EC	Signals and Systems	3	1	0	4
6.	PC 304 EC	Network Analysis and Synthesis	3	0	0	3
7.	MC-220	Constitution of Indian	2	0	0	0
8.	PC 351 EC	Electronics Devices and Circuits Laboratory	0	0	3	1.5
9.	PC 352 EC	Digital System Design Laboratory	0	0	3	1.5
Total			**18**	**3**	**6**	**24**

L : Lectures
T : Tutorials
P : Practical’s
CIE : Continuous Internal Evaluation
SEE : Semester End Examination
BS : Basic Sciences
ES : Engineering Sciences
PC : Professional Core
HS : Humanities and Social Sciences

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Department of Electronics & Communication Engineering

B. Tech. (ECE) III SEMISTER
BSC-105
Mathematics - III

Statistics, Probability, and Numerical Techniques

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 30
3	0	0	3	External Marks: 70

Module1: Statistical Methods

Introduction, Collection of Data, Graphical Representation, Measures of Dispersion, Moments, Skewness, Kurtosis, Correlation, Coefficient of Correlation, Lines of Regression.
(Sections 25.1, 25.2, 25.3, 25.6, 25.9, 25.10, 25.11, 25.12, 25.13, 25.14 of Text Book)

Module2: Probability & Distributions

Probability, Addition Law of Probability, Independent Events, Baye's Theorem , Random Variable, Continuous Probability Distribution, Expectation, Moment Generating Function, Binomial Distribution , Poisson Distribution, Normal Distribution, Exponential Distribution. (Sections26.1,26.4,26.5,26.6,26.7,26.9,26.10,26.11,26.14,26.15,26.16,26.19(6) of Text Book)

Module3: Numerical Techniques-I

Solution of Algebraic and Transcendental Equations, Principle of Least Squares, Method of Least Squares, Fitting of Other Curves, Finite Differences, Forward Differences, Backward Differences. (Sections 28.2, 24.4, 24.5, 24.6, 30.2, 30.2(1), 30.2(2) Of Text Book)

Module4: Numerical Techniques-II

Central Differences, Other Difference Operators, Newton's Interpolation Formulae, Gauss's Forward Interpolation Formula, Interpolation with Unequal Intervals, Numerical Differentiation. Sections 29.7, 29.4, 29.6, 29.7(1), 29.9, 30.1.of Text Book)

Module5: Numerical Techniques-III

Numerical Integration, Trapezoidal Rule, Simpson's one –third Rule, Simpson's three-eight Rule, Weddle's Rule, Solution of Simultaneous Linear Equations (Iterative Methods)
(Sections 30.4, 30.6, 30.7, 30.8, 30.10, 28.5 of Text Book)

Text Book:

B.S Grewal, Higher Engineering Mathematics, 43rd Edition, Khanna Publications.

References

1. Erwin Kreyszig, Advanced Engineering Mathematics, 8th Edition, John Wiley & Sons
2. S.C. Gupta, V.K. Kapoor, Fundamentals of Mathematical Statistics, Sultan Chand &Sons
3. S.S. Sastry, Introductory Methods of Numerical Analysis, PHI Learning Pvt. Ltd.

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Department of Electronics & Communication Engineering

B. Tech. (ECE) III SEMISTER
HS 901 MB
MANAGERIAL ECONOMICS AND ACCOUNTANCY

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 30
3	0	0	3	External Marks: 70

UNIT – I

Meaning and Nature of Managerial Economics: Managerial Economics and its usefulness to Engineers, Fundamental Concepts of Managerial Economics-Scarcity, Marginalism, Equimarginalism, Opportunity costs, Discounting, Time perspective, Risk and Uncertainty, Profits, Case study method.

UNIT – II

Consumer Behavior: Law of Demand, Determinants, Types of Demand; Elasticity of Demand (Price, Income and Cross-Elasticity); Demand Forecasting, Law of Supply and Concept of Equilibrium. (Theory questions and small numerical problem can be asked).

UNIT – III

Theory of Production and Markets: Production Function, Law of Variable Protection, ISO quants, Economics of Scale, Cost of Production (Types and their measurements), Concept of Opportunity cost, Concept of Revenue, Cost-Output relationship, Break-Even Analysis, Price-Output determination under perfect Competition and Monopoly (Theory and problems can be asked).

UNIT – IV

Capital Management: Significance, determination and estimation of fixed and working capital requirements, sources of capital, Introduction to capital budgeting, methods of payback and discounted cash flow methods with problems. (Theory questions and numerical problems on estimating working capital requirements and evaluation of capital budgeting opportunities can be asked).

UNIT – V

Book-keeping: Principles and significance of double entry book keeping, Journal, Subsidiary books, Ledger accounts, Trial Balance, concept and preparation of Final Accounts with sample adjustments, Analysis and interpretation of Financial statements through Ratios.
(Theory questions and numerical problems on preparation of final accounts, cash book, pretty cash book, bank reconciliations statement, calculation of some ratios).

Suggested Readings:

1. Mehta P.L., *Managerial Economics-Analysis, Problems and Cases*, Sulthan Chand & Sons Educational Publishers, 2011.
2. Maheswari S.N., *Introduction to Accountancy*, Vikas Publishing House, 2005.
3. Pnadey I.M., *Financial Management*, Vikas Publishing House, 2009.

Faculty of Engineering & Technology
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B. Tech. (ECE) III SEMISTER
PC 301 EC
ELECTRONICS DEVICES AND CIRCUITS

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 30
3	1	0	4	External Marks: 70

UNIT –I

Semiconductor Diode: Qualitative Theory of P-N Junction, P-N Junction as a Diode, Diode Equation, Volt-Ampere Characteristics, Temperature dependence of V-I characteristic, Ideal versus Practical – Resistance levels (Static and Dynamic), Transition and Diffusion Capacitances, Diode Equivalent Circuits, Load Line Analysis, Breakdown Mechanisms in Semiconductor Diodes, Zener Diode Characteristics and Applications.

UNIT-II

Semiconductor Diode Applications: Half wave, Full wave and Bridge rectifiers – their operation, performance characteristics and analysis. Filters (L, C, LC and CLC filters) used in power supplies and their ripple factor calculations, design of Rectifiers with and without Filters.
Special Diodes (Qualitative Treatment only): Tunnel Diode, Varactor Diode, Schottky Diode, Light Emitting Diode, Photo Diode and Solar cells.

UNIT-III

Bipolar Junction Transistor: Transistor Junction formation (collector-base, base-emitter Junctions), Transistor biasing – band diagram for NPN and PNP transistors, current components and current flow in BJT, Ebers moll model, Modes of transistor operation, BJT V-I characteristics in CB, CE, CC configurations, BJT as an amplifier, BJT biasing techniques, operating point stabilization against temperature and device variations, Bias stabilization and compensation techniques, Biasing circuits design.

UNIT-IV

Small Signal Transistors equivalent circuits: Small signal low frequency h-parameter model of BJT, Approximate model, Analysis of BJT amplifiers using Approximate model for CB, CE and CC configurations; High frequency - Π model, Relationship between hybrid -Π and h – parameter model.

UNIT-V

Junction Field Effect Transistors (JFET): JFET formation, operation & current flow, V-I characteristics of JFET,

MOSFETs: Enhancement & Depletion mode MOSFETs, current equation, V-I characteristics, DC-biasing, Low frequency small signal model of FETs. Analysis of CS, CD and CG amplifiers, MOS Capacitor.

Suggested Reading:

1. Jacob Millman, Christos C. Halkias, and Satyabrata Jit, "Electronic Devices and Circuits", 3rd ed., Mc-Graw Hill Education, 2010.
2. Robert Boylestad and Louis Nashelsky, Electronic Devices and Circuit Theory, 11th ed., Pearson India Publications, 2015.
3. Salivahanan.S, Suresh Kumar.N "Electronic Devices and circuits", 3rd edition, Tata McGraw-Hill, 2012.

Faculty of Engineering & Technology
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B. Tech. (ECE) III SEMISTER
PC 302 EC
DIGITAL SYSTEM DESIGN

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 30
3	1	0	4	External Marks: 70

UNIT-I
Number System and Logic Simplification: Number Systems, Base Conversion Methods and Complements of Numbers. Review of Boolean algebra and De Morgan's Theorem, SOP & POS forms, Canonical forms, Karnaugh map up to 5 variables, Tabular method.

UNIT-II
Combinational Logic Design: Half and Full Adders, Subtractors, Serial and Parallel Adders, BCD Adder, Barrel Shifter, ALU, Comparators, Multiplexers, De-multiplexers, Encoder, Decoder, Driver & Display Devices, Code Converters.

UNIT-III
Sequential Logic Design: Building blocks like S-R, JK and Master-Slave JK Flip-flops, D and T Flip-Flops. Ripple and Synchronous Counters, Shift Registers, Finite State Machines, Design of synchronous FSM, Algorithmic State Machine charts. Designing synchronous circuits like Pulse train generator, Pseudo Random Binary Sequence generator, Clock generation.

UNIT-IV
Logic Families: Design of TTL Logic family, Specifications, Noise margin, Propagation delay, fan-in, fan-out, Tristate TTL, ECL, CMOS Logic families and their interfacing. Logic implementation using PLDs-PROM, PAL and PLA. Introduction to CPLD and FPGA.

UNIT-V
Verilog HDL: Introduction to HDL, Verilog HDL Basics: Module Concept, Lexical Conventions, Value Set, Constants, Data Types, Primitives, Module modeling styles: Structural, Data flow and Behavioral.

Suggested Reading:

1. R.P.Jain, "Modern Digital Electronics", Tata McGraw Hill, 4th Edition, 2009.
2. M.Morris Mano, Michael D. Ciletti, "Digital Design", Pearson, 4th Edition, 2012.
3. Ming-Bo Lin, "Digital System Design and Practices Using Verilog HDL and FPGAs", Wiley India Pvt. Ltd., 2012.

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Department of Electronics & Communication Engineering

B. Tech. (ECE) III SEMISTER
PC 303 EC
SIGNALS AND SYSTEMS

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 30
3	1	0	4	External Marks: 70

UNIT-I
Introduction to Signals & Systems: Classification of signals, Operations on signals, types of systems, Exponential and Trigonometric Fourier series, Dirichlet's condition.

UNIT-II
Fourier Transform: Representation of aperiodic signal, Introduction of Fourier transform, Convergence, properties of Fourier Transform, Fourier transform of periodic signals, Singularity function, Parseval's theorem, Energy spectral density, Development of Discrete Time Fourier transform, Convergence issues associated with the DTFT.

UNIT-III
Sampling: Sampling of continuous time signals, sampling theorem, Aliasing effect, reconstruction of a signal and its samples.
Convolution & Correlation of signals: Convolution integral, Properties of convolution, Graphical method of convolution, Convolution of Discrete time signals, overlap-add and overlap-save method of discrete convolution, Definition of correlation, Auto correlation, Properties of Autocorrelation, Cross correlation of signals.

UNIT-IV
Laplace Transform: Review of Laplace transforms, region of convergence and properties, poles and zeros, relation between Laplace and Fourier transforms, properties of Laplace transform, inverse Laplace transform, Solutions to differential equation and system behavior.

UNIT-V
Z Transform: Definition of Z-Transform, Properties of Z-Transform, Region of convergence of Z-Transform, Inverse Z Transform using Inspection, Partial fraction expansion, Power series Expansion, Contour integration methods, Parseval's relation analysis of discrete time systems using Z-Transform. Realization of discrete time system using Direct form, Cascade parallel forms.

Suggested Readings:

1. Alan V. Oppenheim, Alan. S. Willsky, S Hamid Nawab, *Signals and Systems*, 2nd edition, Prentice Hall of India, 2007.
2. Lathi B.P., *Signals Systems Communications*", 1st edition, B.S. Publications, 2006.
3. Simon Haykin and Van veen, "Signal and system", Willy, second edition.

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B. Tech. (ECE) III SEMISTER
PC 304 EC
NETWORK ANALYSIS AND SYNTHESIS

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 30
3	0	0	3	External Marks: 70

UNIT – I

Network Theorems: Circuit Elements, Dependent and Independent Sources, Passive Elements, R, L, C, Energy Stored in L, C, Wye-Delta transformation, Nodal and Mesh analysis, Tellegen's Theorem and Maximum Power Transfer Theorem.

Network Topology: Graph, Tree, Tie set, cut set matrix, Impedance matrix formulation of node loop equations using tie-set, cut-set analysis.

UNIT – II

Two port networks: Z, Y, h, g, ABCD parameters, equivalence of two ports, Condition for Symmetry and Reciprocity. T-PI transformations, inter connection of two ports networks, Brune's test for interconnection.

UNIT – III

Response of R, L, C Networks: DC and AC excitations of RL, RC and RLC circuits, Transient Analysis. Resonance-Series and parallel. Quality factor, Bandwidth of Resonant Circuits, Steady state sinusoidal analysis using phasors, active power, reactive power and power triangle.

UNIT – IV

Filters and Attenuators and Equalizers: Constant K filters, LP, HP, BPF, BSF, m-derived composite filter design, lattice filters. Symmetrical, Asymmetric T, PI sections networks, Characteristic Impedance, Image Impedances, Iterative Impedance and propagation constant. Design of Attenuators-Symmetrical T, Pi, Lattice and Bridge-T.

UNIT – V

Network Synthesis: Fosters reactance theorems, Positive real function, Hurwitz polynomial, Driving point Impedance and admittance. Synthesis of one port RC, RL and LC networks using Foster and Cauer forms.

Suggested Readings:

1. Van Valkenberg M.E, *Network Analysis*, 3rd edition, Prentice Hall of India, 1996
2. Hayt W H, Kemerly J E Durbin, *Engineering Circuit Analysis*, 7th edition, Tata McGraw Hill, 2006.
3. Smarajit Ghosh, *Network Theory Analysis and Synthesis*, PHI Learning private Limited,2013

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B. Tech. (ECE) III SEMISTER
MC-220
CONSTITUTION OF INDIA

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 30
2	0	0	0	External Marks: 70

UNIT -1

1. Making of Indian Constitution - Constituent Assembly
2. Historical Perspective of the Constitution of India
3. Salient Features and characteristics of the Constitution of India

UNIT -2

1. The Fundamental Rights
2. The Fundamental Duties and their Legal Status
3. The Directive Principles of State Policy – Their Importance and Implementation

UNIT -3

1. Federal Structure and Distribution of Administrative, Legislative and Financial Powers between the Union and the States
2. Parliamentary Form of Government in India – The Constitutional Powers and Status of the President of India
3. Amendment of the Constitutional Provisions and Procedure

UNIT -4

1. The Judiciary
2. Constitutional and Legal Frame Work for Protection of Environmental in Global and National Level
3. Corporate Social Responsibility (CSR) International and National Scenario.

Text books:

1. D.D. Basu: An Introduction of Indian Constitution
2. Greanvile Austin: The Indian Constitution
3. Paras Diwan: Studies on Environmental cases

References books:

1. KhannnaJustice.H.R: Making of India's Constitution, Eastern Book Companies.
2. Rajani Kothari: Indian Politics
3. Ghosh Pratap Kumar: The Constitution of India. How it has been Formed, World Press.
4. A.Agrawal (Ed): Legal Control of Environmental Pollution.

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B. Tech. (ECE) III SEMISTER
PC 351 EC
ELECTRONICS DEVICES AND CIRCUITS LABORATORY

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 25
0	0	3	1.5	External Marks:50

List of Experiments

1. Measurement of static and dynamic resistances of Silicon and Germanium diodes.
2. Zener diode Characteristics and its application as voltage regulator.
3. Design, realization and performance evaluation of half wave rectifiers without and with filters.
4. Design, realization and performance evaluation of full wave rectifiers without and with filters.
5. Static characteristics of Bipolar-junction Transistor CB configuration
6. Static characteristics of Bipolar-junction Transistor CE configuration
7. Design of Self Bias Circuit
8. Drain and Transfer Characteristics of JFET
9. Design of JFET Common Source Amplifier
10. Design of Common Emitter BJT amplifier
11. Characteristics of UJT
12. Simulate any two experiments using PSPICE

Note: A minimum of 10 experiments should be performed

Suggested Reading:

1. Paul B. Zbar, Albert P. Malvino, *Micheal A. Miller*, *Basic Electronics*, *A text – Lab Manual*, 7th Edition, TMH 2001.

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B. Tech. (ECE) III SEMISTER
PC 302 EC
DIGITAL SYSTEM DESIGN LABORATORY

Teaching Scheme				Examination Scheme
L	T	P	C	Internal Marks: 25
0	0	3	1.5	External Marks: 30

List of Experiments

1. Implementation of all logic gates using universal gates
2. Implementation of half adder, full adder, half Subtractor and full Subtractor using universal gates
3. Implementation Boolean functions using suitable multiplexer
4. Design a 4 – bit Adder / Subtractor
5. Design and realization a 4 – bit gray to Binary and Binary to Gray Converter
6. Truth table verification of SR Flip Flop using NAND and NOR gates.
7. Truth table verification of JK, D and T flip flops
8. Shift register implementation using flip flops
9. Synchronous counter implementation using flip flops
10. Truth table verification of asynchronous counters
11. Design of Up/Down counters
12. Realization of logic gates using DTL, TTL, ECL, etc.,

Note: A minimum of 10 experiments should be performed.

Suggested Reading:

1. M.Morris Mano, Michael D. Ciletti, "Digital Design", Pearson, 4th Edition, 2012.